STM JOURNALS

Journal of Instrumentation Technology & Innovations
ISSN: 2249-4731(online), ISSN: 2347-7261(print)
Volume 5, Issue 2
www.stmjournals.com

Design and Implementation of Single-Phase, Three-Level, Sub-Harmonic PWM Inverter with Short-Circuit Fault Detection

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Abstract

This paper investigates the design and implementation of single-phase, three-level inverter controlled by sub-harmonic pulse-width modulation (SH-PWM). The performance of developed 3-level inverter is simulated and then is compared with 2-level conventional inverter as well as FFT analysis. Experimental test has been undertaken to examine the operating characteristics of the implemented inverter for supplying an inductive load. To increase the reliability of designed inverter in different applications, a short-circuit fault detection has been considered. Moreover, to reduce the voltage harmonic contents of the inverter, an LC low-pass filter is employed. Finally, an efficiency analysis is given to show the satisfactory performance of the developed inverter.

Keywords: *Three-level inverter, sub-harmonic PWM (SH-PWM), total harmonic distortion (THD), short-circuit fault detection, LC filter, H-bridge*

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INTRODUCTION

Common conventional three-level or two-level square-wave inverters generate large harmonic in their first components that make a bulk high magnitude harmonic order in 3rd, 5th, 7th, 9th components [1]. Figure 1 shows the harmonic analysis of a three-level square-wave inverter's voltage waveform. On the other hand, a two-level PWM inverter generates non-sinusoidal output voltage waveform.

Taking these problems into consideration and the fact that the multilevel inverters offer better total harmonic distortion (THD) [2], results in three-level PWM modulation strategy have become a point of interest. Pulse-width modulation (PWM) techniques have been widely accepted as a good control strategy for inverters [3].

The main advantages of PWM inverters in comparison to square-wave inverters are: (i) control of voltage magnitude without need to variable DC bus voltage, (ii) reduction of unwanted harmonic voltages, and (iii) improved power factor with unity displacement factor [4]. Lowest order harmonic elimination is possible by proper choice of the number of pulses per half cycle.

The fundamental voltage and the harmonic content can be controlled by using PWM techniques. There exist various waveform synthesis methods, which include space vector PWM modulation [5], sigma delta modulation [6], switching frequency optimal PWM modulation [7] and sub-harmonic PWM (SH-PWM) [8, 9] as applied to three-level inverters.

This paper presents the selection of the switching devices and integrating the circuits that used in the inverter, and implementation details of the inverter are investigated. Experimental tests with an R-L load at full voltage, and maximum rated current have been carried out to evaluate the performance of the three-level inverter.

The results show that the inverter output voltage has three voltage levels and approximately as sinusoidal. Then the output load currents also have low-level harmonic components.

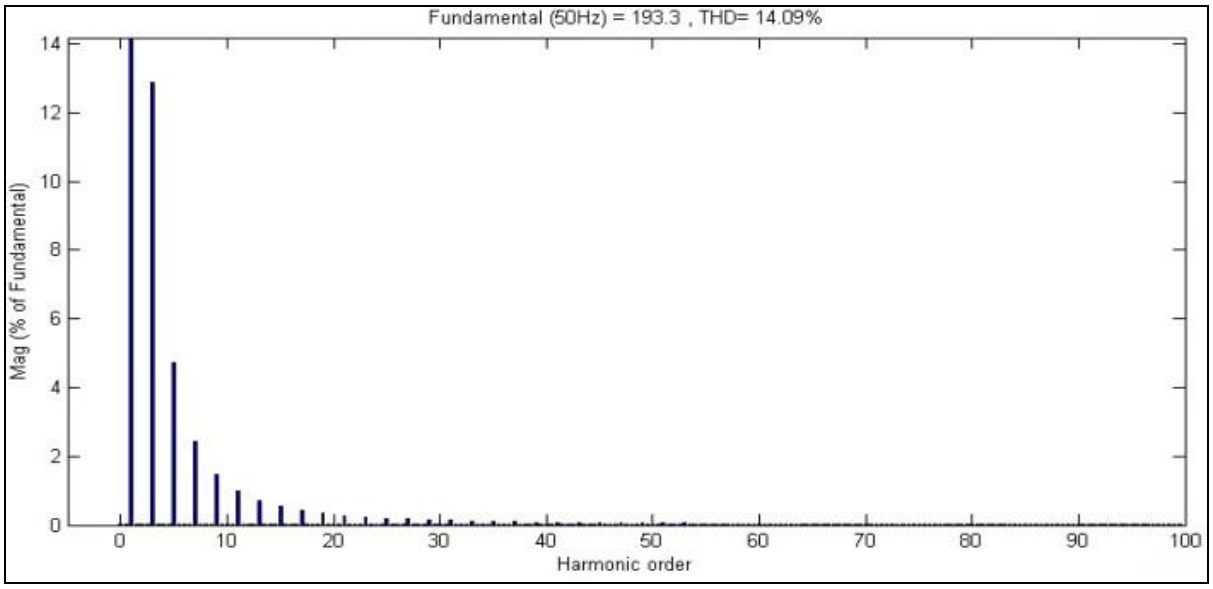

Fig. 1: *Harmonic Analysis of a Three-Level Square-Wave Inverter's Voltage.*

H-BRIDGE SWITCHING DEVICE SELECTION

Figure 2 shows the waveforms of the inverter phase voltage and phase current under steady-state operation with a motor load at the nominal fundamental frequency of 60 Hz. The inverter output voltage has three voltage levels, and the motor current is very close to a sinusoidal waveform. As shown in Figure 2, the steady state RMS value of the inverter output current is about 50 A when the inverter operates with a maximum motor overload at a frequency of 60 Hz. To account for overload current transient conditions, the current rating of the switching device should be at least 1.5 times the value of the steady-state current [10]. Thus, the overload rating of the switching device should be at least 50 A. Therefore, each switch should have at least a peak current rating of about 75 A.

The three-level inverter operates from a nominal 240 V DC power supply. According to the simulation results, the voltage stress experienced by each switching device is limited to half the total DC bus voltage or 120 V. To allow an adequate voltage margin for inductive di/dt voltage spikes, switching devices with at least a blocking voltage rating of 200 V need to be chosen. IGBTs are the modern efficient switching elements for medium power inverter applications [11]. Typically, the closest available IGBT devices have a current rating of 150 A. At this current rating, the blocking voltage rating of the device is usually 600 or 1200 V. Therefore, IGBT devices with rating of 150 and 600 V are chosen for best performance in high-power source inverters for three-phase usages. For experimental tests and medium output voltage, power MOSFETs that are originally designed for low or medium power in low power full-bridge inverter applications are used due to their lower cost. With parallel three modules can be obtained the required 150 A rating. TL494 ICs are used in the inverter as the PWM signal generator. These ICs have internal saw-tooth wave generator and comparator block that satisfies operating requirements and reduces the physical circuits.

For the selected IGBT module, the temperature coefficient of V_{CE} (sat) goes from a bipolar-like negative at low current to a MOSFET-like positive coefficient as current increases above its rated value [12]. At high current levels, the behavior is similar to the power-MOSFET and current balance between devices improves when the temperature difference increases. Therefore, the minor differences occurring between the V_{CE}(sat) of parallel dies are automatically balanced with small temperature variations. Figure 3 shows single-phase of the three-level inverter. The positive DC input is connected to the drain of the top switches module, and the negative DC input is connected to the source of the bottom power MOSFET module [13]. The gates of the switches are energized by two SH-PWM gate drive signals via resistor.

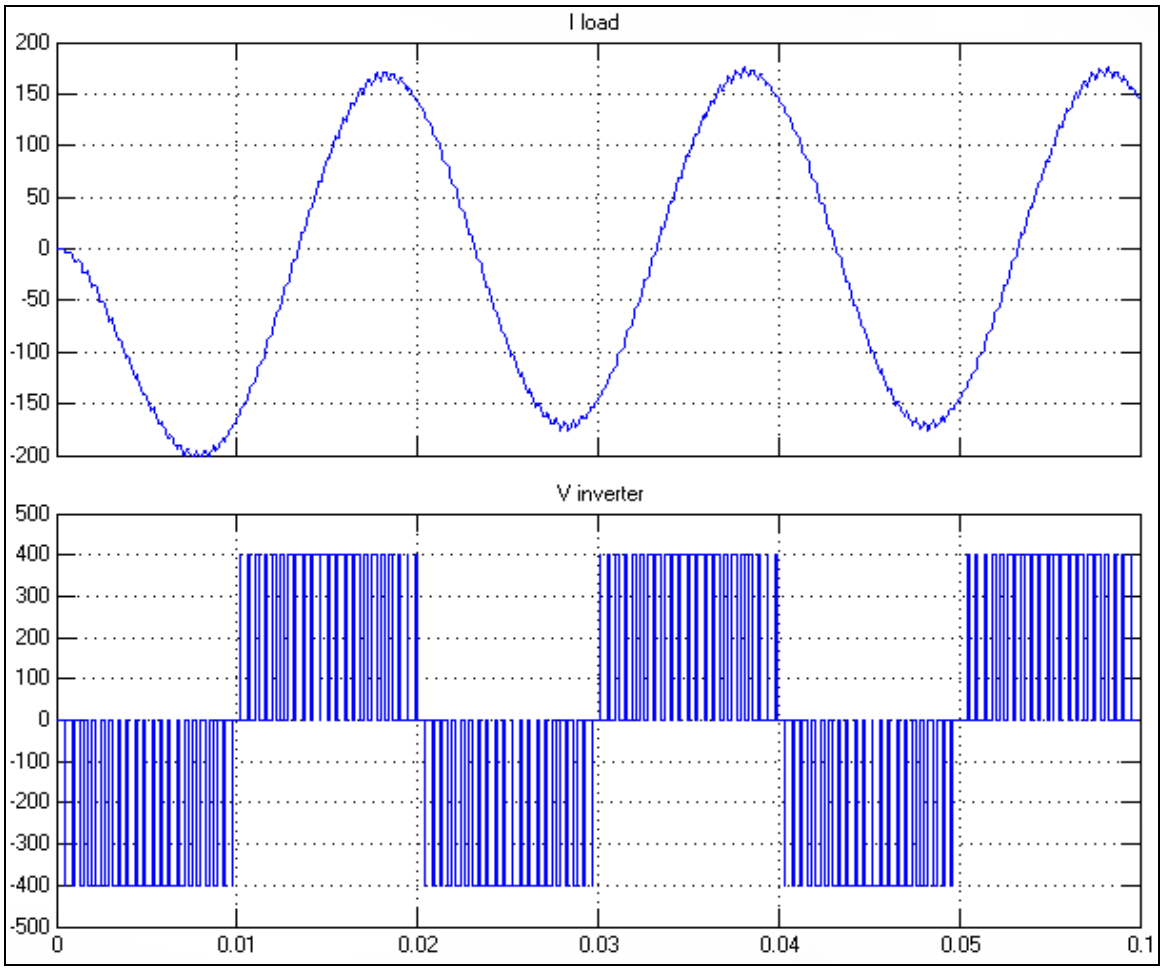

Fig. 2: *Phase Voltage and Phase Current Waveforms for Fundamental Frequency of 60 Hz.*

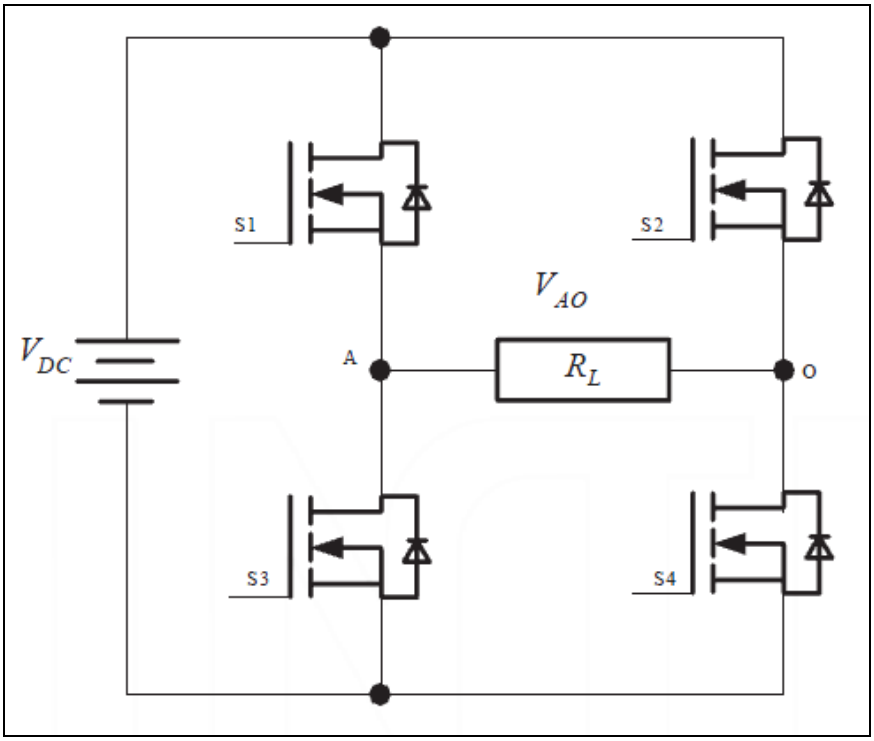

Fig. 3: *One-Inverter Leg of Full-Bridge Three-Level Inverter.*

DETERMINATION OF THE INVERTER SPECIFICATION

To demonstrate the performance of a three-level inverter, steady state operation of inverter with an inductive load is simulated. Based on the simulation circuit diagram shown in Figure 4, the load is modeled as an inductor-resistor load. The values as load inductor and resistor are chosen as 5 mH and 1 Ω in order to produce similar current waveforms as drawn by an induction motor load. The DC bus voltage is constant at 400 V. The single-phase, three-level inverter with foregoing inductive load is simulated as shown in Figures 4 and 5 shows FFT frequency spectrum of three-level phase voltage of Figure 2. The magnitude of the harmonic components is calculated up to the 100th harmonic (40 kHz). The numbers correspond to the harmonic order, where the number 1 is the fundamental. In the case of the three-level inverter, harmonic components of harmonic order 40–50 either side of which are around the switching frequency, are the largest. They are less than 1% of the fundamental component. According to simulation results, the total harmonic distortion (THD) of output current in three-level inverter is 1.37%. When comparing square-wave output of three-level inverter shown in Figure 1 and output of three-level PWM inverter shown in Figure 5, it is clear that the PWM pushes the harmonics into a high-frequency range around the switching frequency FC [4]. With comparing of Figures 5 and 6, the significant harmonic reduction in three-level PWM inverter can be concluded. The advantages of three-level inverter are good power quality, low switching losses, reduced output dv/dt and high voltage capability. Increasing the number of voltage levels in the inverter increases the power rating.

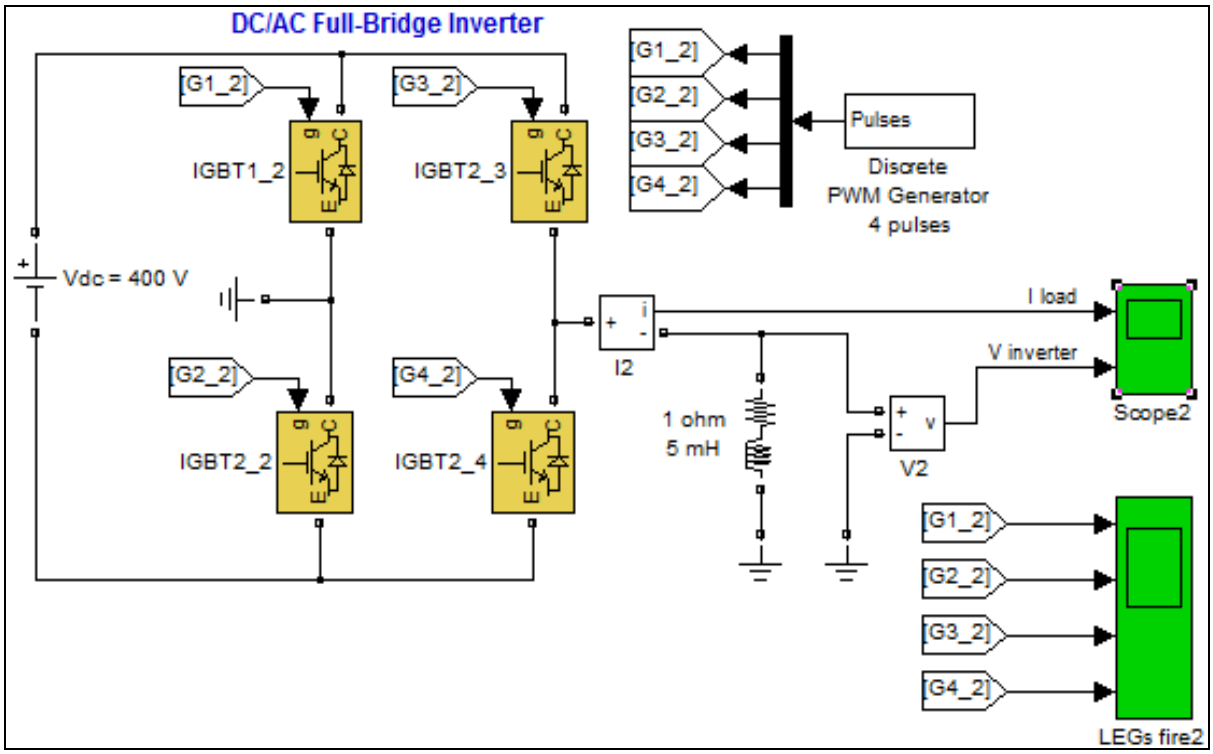

Fig. 4: *Simulation Block Diagram of Single-Phase Three-Level Inverter.*

INVERTER CONSTRUCTION AND FAULT DETECTION

The control principle of the SH-PWM method for a three-level is based on the use of two triangular carrier waveforms with one reference signal per phase [9]. The input reference is compared against two carriers and the crossover instance of the input reference voltage with the corresponding carrier waveform gives the switching instance for the particular level. SH-PWM is the most popular control technique for inverters because of its simplicity [9]. The SH-PWM method is selected for this investigation of a three-level inverter. One three-level inverter, SH-PWM control signal schematic is shown in Figure 7.

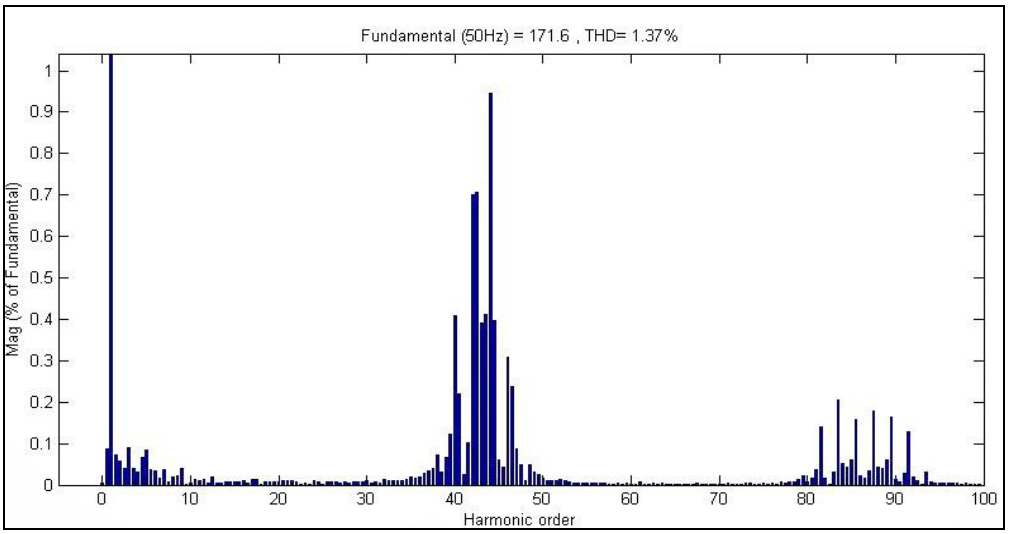

Fig. 5: *Frequency Spectrum of Simulated Three-Level Inverter.*

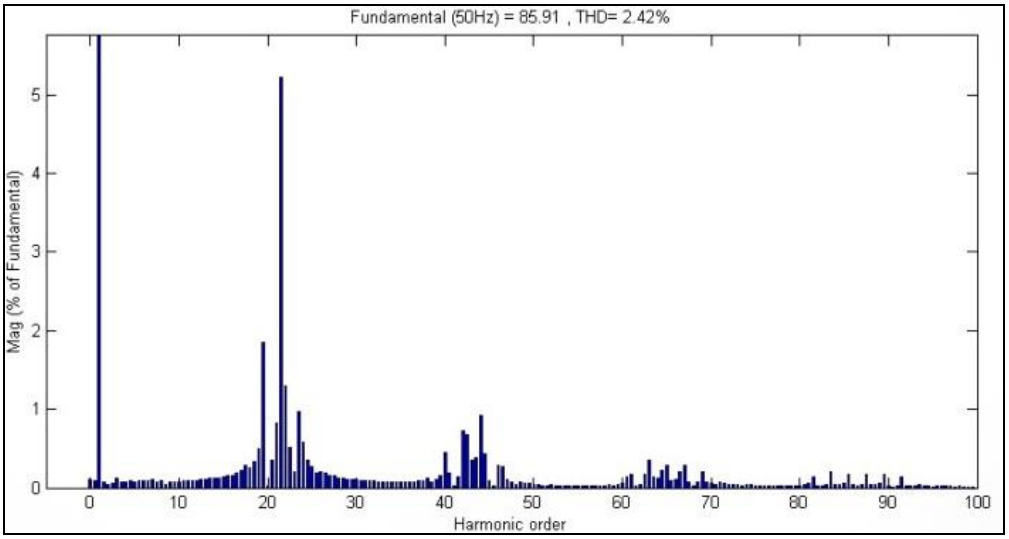

Fig. 6: *Frequency Spectrum of Simulated Two-Level Inverter.*

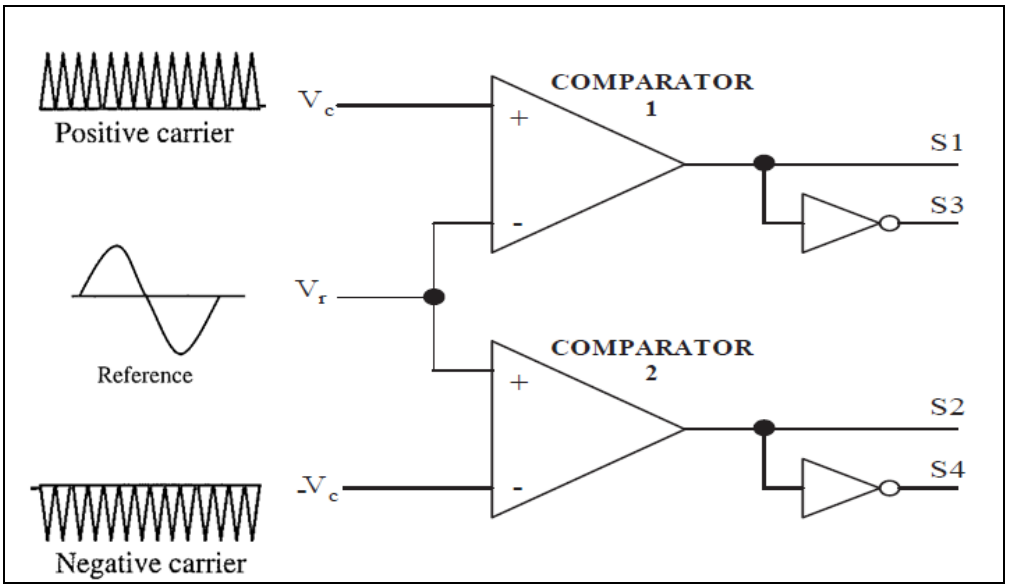

Fig. 7: *SH-PWM Control Signal Schematic.*

The TL494 generates a PWM signal by comparing an internally generated saw-tooth wave with an error signal that must be a reference half-sine wave. Common applications for this chip are DC/DC converters, where an output voltage is programmed by resistors in the error feedback path that is referenced to some DC voltage signal. In make out DC/AC converter, must use the error amplifiers with no feedback from the output so that the error signal is the signal we want encoded in the SH-PWM output. Two half-rectified sine waves that are equal in amplitude and 180° out of phase compared to each other input to TL494 for internal comparator and finally make SH-PWM control signal to drive switching devices in full-bridge section. For support, full-bridge power MOSFET leg must use two SH-PWM generators. This means that two of TL494 ICs must be involved in this project. TL494s programmed a switching frequency of 40 kHz with $R = 25\ k\Omega$ and $C = 1000$ pF. Figure 8 shows one of the outputs of SH-PWM signal generator controller. The high-voltage fast diode D1 (FR105) is used as a fault-sensing element. The blocking voltage rating of the diode FR105 is 600 V and sufficient to sustain the high DC bus bar voltage. If the IGBT is turned on into an existing short condition, V_{CE} remains at its off state levels as the main supply voltage is forced across the collector and the emitter terminals. For protection stage, the diode D1 FR105 becomes reverse-biased and the MOSFET M1 (BUZ11A) begins to be charged as the MOSFET gate voltage rises and the MOSFET will start to be turned on. This causes the IGBT gate signal to be clamped to a lower voltage of its active voltage (ex. 9 V from 15 V) and IGBT is turned off completely. Figure 9 demonstrates these processes. Output of H-bridge is ideally a 60 Hz sine wave with a vrms of 90–130 V. Because it is encoded using a 40 kHz SH-PWM signal, it must be filtered. Due to the high voltage of the output, the only option is a passive filter, which is an inductor and capacitor in series (Figure 10), with the load connected across the capacitor.

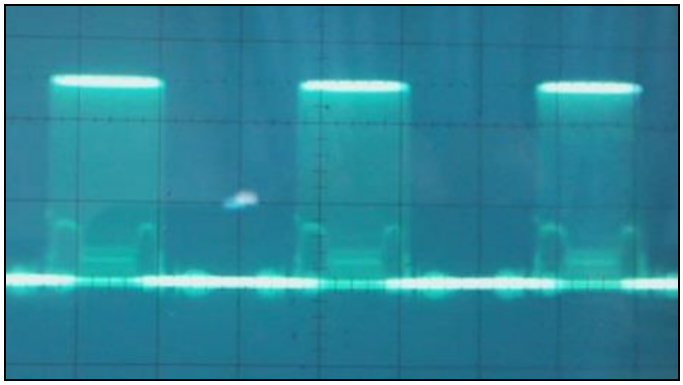

Fig. 8: *SH-PWM Signal Output of TL494.*

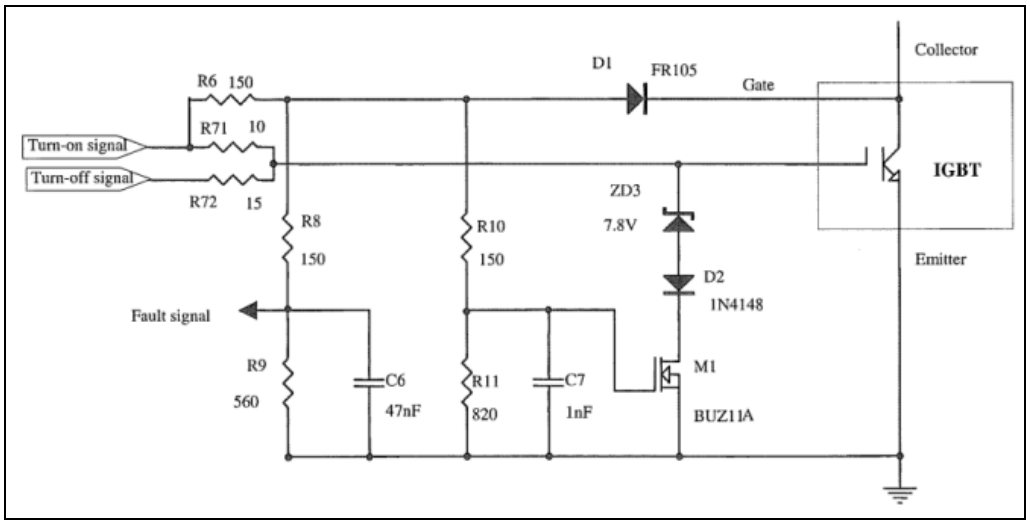

Fig. 9: *Protection Circuit.*

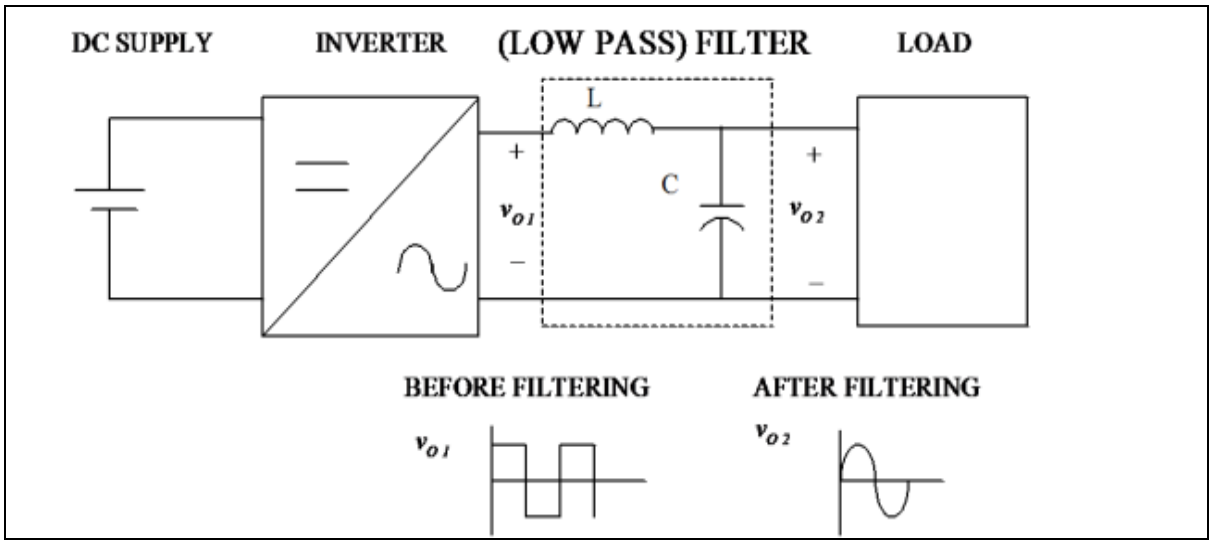

Fig. 10: *Passive Filter (Series L-C Filter).*

In this implementation, optimal desired a cut-off frequency comfortably below switching frequency and above ideal 60 Hz output. In an L-C filter, the cutoff frequency is given by the relationship using a capacitor of 14 μF and an inductor of 33 μH, with calculations is obtained a cutoff frequency of 7.153 kHz.

$$f_c = \frac{1}{\sqrt{LC} * 2\pi} \Rightarrow f_c = \frac{1}{\sqrt{33\mu H * 14\mu F} * 2\pi}$$
$$= 7.404\,\text{kHz}$$

This inverter also needed components that are capable of handling the rated voltage and current output of system, so we needed an inductor, which could handle at least 2 A, and a capacitor which could handle at least 170 VAC. To this end, the inductor, which is rated for 5–20 A and the capacitor, which is rated for 275 VAC, have been selected.

TEST RESULTS

This single-phase three-level SH-PWM inverter was initially constructed and tested with 130 V DC voltage source to demonstrate its operation. The test is performed with a fundamental frequency of 400 Hz, a switching frequency of 44 kHz, and DC-link voltage of 130 V. Figure 11 shows the inverter test result.

The gate-drive frequency-controlled method SH-PWM, uses high switching frequency (up to 44 kHz) to filtering the output so that after passing this output voltage through an LC filter, this makes a pure sinusoidal output voltage and current waveforms and total harmonic distortion will be less than 15%. Figure 12 shows the filtered output voltage.

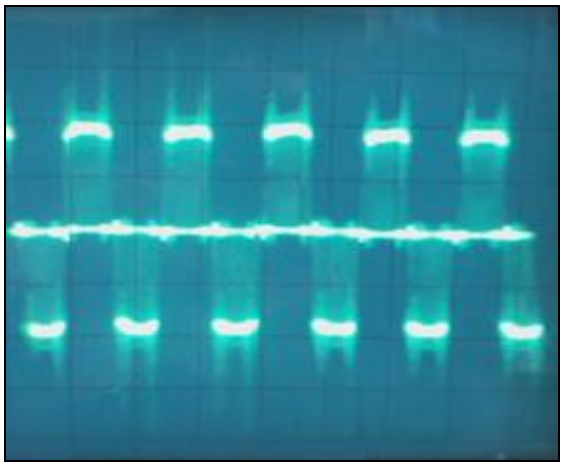

Fig. 11: *Unfiltered Output Voltage Waveform of a Three-Level Inverter.*

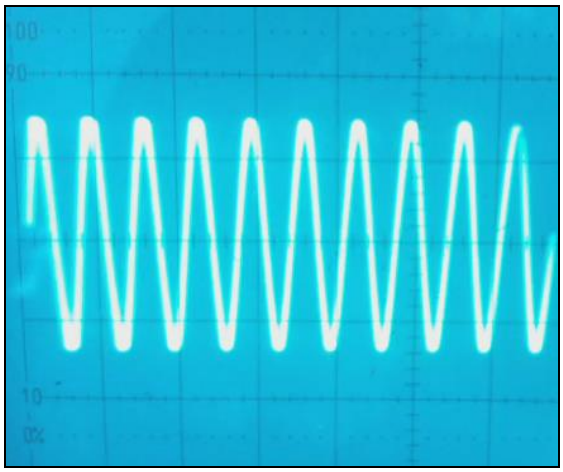

Fig. 12: *Filtered Output Voltage Waveform of a Three-Level Inverter.*

Another test with oscilloscope was tested at low voltage (Figure 13), with a 16 VDC battery supplying both the H-Bridges, at standard 60 Hz frequency. Using this source, the inverter was connected to a 16 VDC car headlight as a load, with a low-voltage filter of the same value as that described in the previous section.

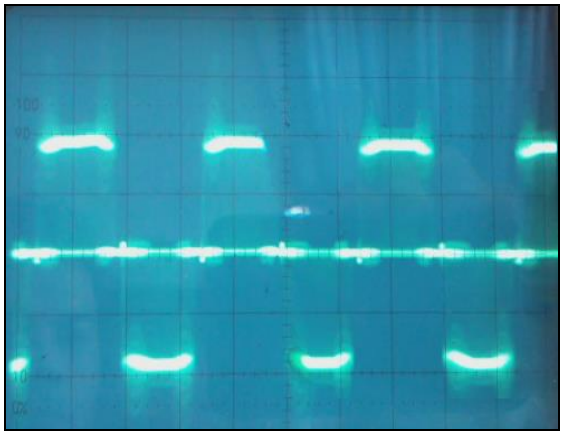

Fig. 13: *Unfiltered Output Voltage.*

The filtered waveform across the 16 VC headlight load has been shown in Figure 14. The output of this low-voltage test shown in Figure 14 is nearly ideal, with very little distortion. This verifies that this three-level SH-PWM inverter generated PWM signal did indeed encode a sine wave, which is sufficiently free of distortion.

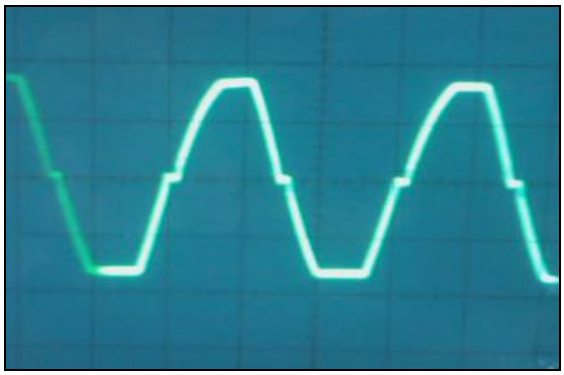

Fig. 14: *Filtered Output Voltage.*

Power Efficiency

In order to determine the power losses, and therefore the efficiency of inverter design, the power into and out of the inverter were experimentally determined for an experimental load. In order to determine the powers, this needed to determine first the voltage and current at the two points. Voltage was a simple matter of using a digital multimeter to measure the voltage of the H-bridge, and again to measure the RMS voltage of the output voltage waveform. In order to determine the currents, though, this needed to use an indirect measurement, using a known resistance in-line with the circuit, and measuring the voltage drop across this resistance. This allowed us to calculate the current going into and out of inverter. The results of these measurements are shown in Table 2.

Table 1: *Power Value and Power Efficiency.*

	V in/out	Resistance	V drop	Current	Power
Input	130 VDC	0.05	0.11 VDC	2.2 ADC	286 W
Output	91.55 Vrms	0.017	0.046 Vrms	2.76 Arms	252 W

Using these values, we can calculate a power efficiency of 88% for this inverter, which is well within the design specifications of efficiency $\geq$ 75%. It should be noted that this power efficiency is for the unfiltered output. Using the LC filter discussed earlier reduces the power output considerably, burning far too much energy as heat in the MOSFETs of the H-bridge.

At this point, the exact cause of this is unknown, and is still being investigated. The value shown in Table 1 is for experimental tests and can increase up to 2200 W for output power.

CONCLUSIONS

A single-phase three-level IGBT/Power MOSFET inverter for an electric automotive with capability converted to a three-phase three-level inverter has been developed. Parallel-pack 600 V/50 A IGBT modules were selected as the main switching elements for the inverter. By paralleling three IGBTs together in each module, the required current rating of 150 A was obtained and a power efficiency of 88% for this inverter calculated. The recommended laminated layer bus bar structure of the inverter permits a compact and clearly arranged mechanical construction. Tests were performed with a simulated induction motor load with R-L-C components

at full voltage, and maximum rated current. The results showed that the inverter is capable of reliable and efficient operation over a range of frequencies. By using inverter in three-phase three-level application this can reach by an extra circuit that create three different sine wave references that are equal in amplitude and 120 ° out of phase compared to each other for gate SH-PWM signal generator has been considered.

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Cite this Article
Niasar Abolfazl Halvaei, Khoei Behzad Habibzadeh. Design and implementation of single-phase, three-level, sub-harmonic PWM inverter with short-circuit fault detection. *Journal of Instrumentation Technology and Innovation*. 2015; 5(2): 5–13p.