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A New Resonant Capacitor Diode Voltage Multiplier Topology for Pulsed Power Application

Today, the pulsed power systems have been employed in many applications. To meet the requirement of user, the pulse generator should enjoy the advantages of compactness, high flexibility, high pulse repetition rate and cost efficiency. Among all of converters that can be used to generate high voltage pulses, capacitance diode voltage multiplier (CDVM) is a good candidate to meet the mentioned requirements. In this paper a new converter that is combination of full-bridge inverter, CDVM and resonant circuit is proposed. The performance of developed converter is compared with the conventional circuits and is demonstrated via simulation in MATLAB/SIMULINK. Experimental tests on a prototype setup have verified the capability of this topology.

Keywords: pulsed power system; capacitor diode voltage multiplier; resonance converter; full-bridge inverter.

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1. Introduction

Pulsed power generators (PPG) are generators that can produce high voltage pulse in a very short time. Today, pulsed power systems (PPS) have found wide applications. These systems are used in medicine, water and air cleaning, food treatment, forming of metals, production of nano-powder, etc. One of the most important components of PPG are closing or opening switches that used to generate the pulse and apply it to load. In the structure of the different generators various switches are used. Generators that use power semiconductor switches, due to compactness, high pulse repetition rate, high reliability, high flexibility and long-life are under special attention[1-3]. This generator can be classified in four categories.

- The generators that use simple structure of storage and switch to discharge energy; in [4], for example, the authors use two large storage capacitors for positive and negative pulses. Two switches are also needed each of which is composed of multiple IGBTs connected in series.
- Marx generators; this structure also make the base for a lot of research on the use of semiconductor switches. Compact Marx generator in [5] has multiple circuit of different discharge frequencies in parallel to generate flat shape pulses. The generator in paper [6] is a simple semi-conductor Marx generator with four stages and its each stage switches are MOSFETs. To increase the blocking voltage capability of each stage in Marx generator a series connection of the devices could be used. The voltage distribution must be controlled either actively or by passive elements [7]. The base of topology used in [8] is also a completely solid-state Marx type circuit using a full-bridge (FB) switch-capacitor cells (SCCs) series connection.

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• DC-DC boost converters; different topologies of dc-dc converters are also candidates for semiconductor pulse generator. In [9], series and parallel connections of fly back converters are used to improved power rating and pulse rise time. Article [10], has used dc-dc converter based on Φ inverter and with the help of a matching network could reduce voltage stress on the switch.

• Capacitor diode voltage multiplier (CDVM); CDVMs due to low voltage stress on diodes and capacitors, being compact, simple structure, and low-cost are options for high voltage applications [11, 12]. The base of performance of these inverters is charging the capacitors by low input voltage in a specific time interval and discharging the stored energy to the load in a short time. Papers [13] and [14] have used power electronic switches in the CDVM structure to create high voltage pulses with high frequency. A combination of a boost DC-DC converter with CDVM is also proposed that fed by AC low voltage and low frequency for water treatment application [12]. In [13] the authors have proposed a new topology of CDVM by adding semiconductor switches in CDVM circuit. In this topology that fed by AC grid, in discharging mode, a number of capacitors in CDVM circuit are connected in series. In [15] the H-bridge inverter is used along with CDVM. The aim of this research is to improve rise time and decay response time. Some article use a combination of other power electronic converter with CDVM in none pulsed power applications to provide a very high voltage gain[16, 17].

The base of the topology in this paper, according to unique features such as simple structure, being compact and very low price, is CDVM. There are different topologies for CDVM. A sample of CDVM circuit is shown in Fig. 1. Moreover, the use of resonance due to the operation of high frequency with soft switching can improve the size and performance of the topology [18, 19, 20, 21]. [18, 19] proposed and designed voltage multipliers with resonance topology for none pulsed power applications. In article [20], an LC resonant circuit is designed that is fed with a full-bridge converter and a CDVM converter is connected in parallel to the capacitor of LC circuit to improve circuit operation and use zero current switching. [21] is another research in which a new topology is proposed by combination of CDVM with resonant circuit. In this topology also the number of CDVM's capacitors are connected in series during discharging mode. Topology of [21] used resonant circuit in any stage to generate wide pulses combined with narrow pulses.

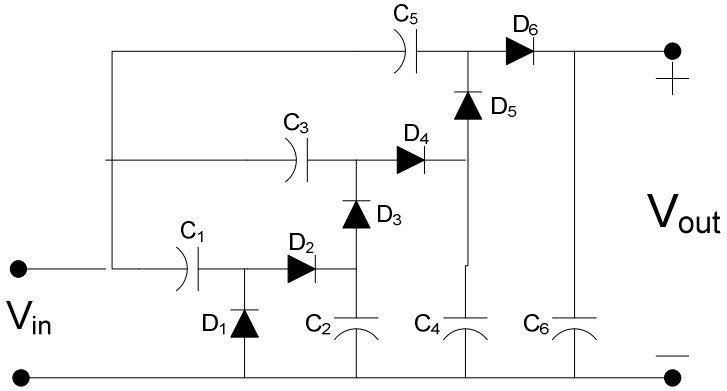

Figure 1. A sample of CDVM circuit

Resonance CDVM topology can contain tiny-size resonant series inductors instead of

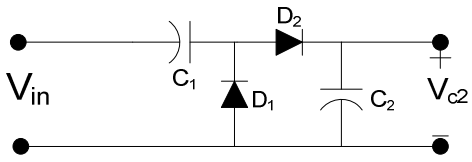

Figure 2. An one stage CDVM

energy storage inductor[19].

In this paper, firstly the performance of a simple CDVM circuit fed by grid voltage is expressed and a simple resonant circuit is assessed. Then, the new topology based on resonance of an inductor with the capacitors in the CDVM circuit is introduced. With simulation in MATLAB, Its performance is compared with the simulation result of simple CDVM circuits fed by Sinusoidal voltage, simple CDVM fed by full-bridge inverter and, CDVM connected to the resonance LC circuit. The elements of CDVM circuits have the same values in all simulations.

2. Basic Circuits

2.1. Capacitor diode voltage multiplier

Fig. 2 shows one stage CDVM circuit. The results of this circuit can be expanded to a circuit with more stages. For simplicity, the capacity of capacitors is considered as the same. Fig. 3(a) shows the equal circuit at the positive half cycle. Assuming zero initial conditions for the capacitor, the capacitors are charged with a positive voltage. As is clear from the circuit of Fig. 3(b) that is the negative half-cycle circuit, C_1 is first discharged and then charged with the reverse polarity. In the next positive half-cycle as indicated in Fig. 3(c), the charging voltage of C_2 is obtained from the following equation:

$$V_{C2} = V_{C1.2} + V_{in} \tag{1}$$

In the above equation, $V_{C1,2}$ is the voltage of C_1 at the end of second step. Again, in the negative half-cycle, the capacitor C_1 is charged with reverse polarity and this trend continues until the voltage of C_2 is twice of the maximum input voltage.

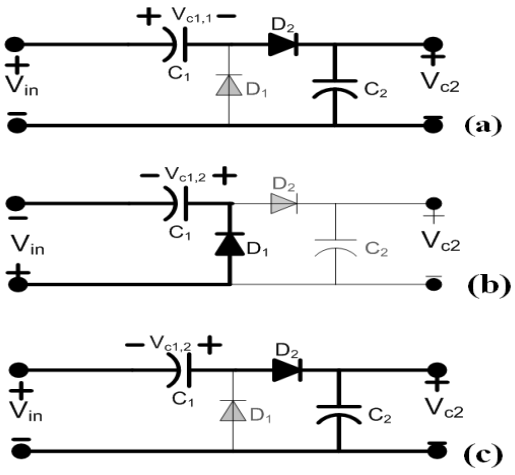

Figure 3. The one stage CDVM in (a)first positive cycle, (b) negetive cycle and, (c) the second positive cycle

2.2. Resonant Circuit

Fig. 4(a) shows a series resonant circuit with diode. When the switch is connected, the inductor current and capacitor voltage are obtained from (2) and (3) respectively.

$$I_L(t)=\sqrt{\frac{C}{L}}V_{dc}\sin(\omega_0 t) \tag{2}$$

$$V_C(t)=V_{dc}(1-\cos(\omega_0 t)) \tag{3}$$

$$\omega_0=\frac{1}{\sqrt{LC}} \tag{4}$$

In the above equations, V_C, I_L and, w_0 are the capacitor voltage in v, inductor current in A and, resonant frequency in rad/s respectively.

Assuming initial zero conditions, Fig. 4(b) shows the capacitor voltage and inductor current. It is clear that at t= $\pi\sqrt{LC}$, capacitor voltage will be twice as the input source and inductor current will be zero. At this moment the diode is turned off and does not allow negative current to pass. Thus, the capacitor voltage after $\pi\sqrt{LC}$ seconds reaches double the supply voltage and remains constant.

3. Resonant CDVM

Fig. 5 shows the schematic of the proposed resonant CDVM, and Fig. 6 shows a simple circuit of the converter discussed in the following part. The results can be extended to more stages. The circuit in Fig. 6 has two switching modes that shown in Fig. 7(a) and 7(b).

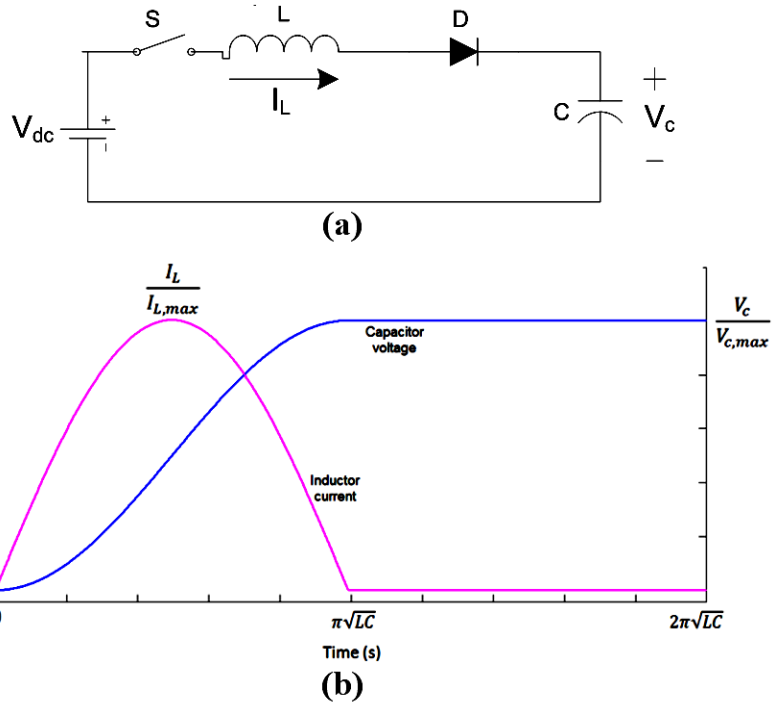

Figure 4. Resonant circuit (a) a simple circuit and, (b) voltage and current

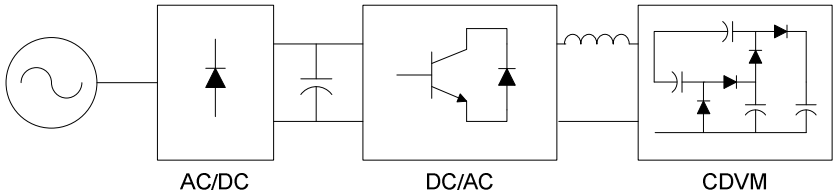

Figure 5. The schematic of proposed topology

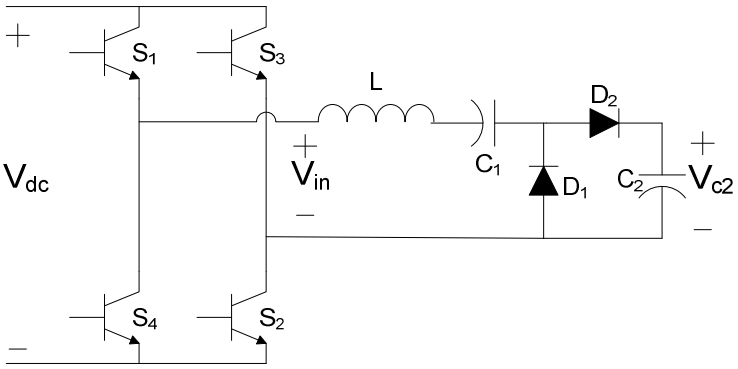

Figure 6. The proposed toplogy with one stage

3.1. The first switching mode 1:

In this mode, switches S_1 and S_2 are on and $V_{in}=V_{dc}$. Equivalent capacity of the capacitors can be obtained from the following equation:

$$C_{eq}=\frac{C_1C_2}{C_1+C_2} \tag{5}$$

Thus, according to (3), assuming $C_1=C_2$, it can be written:

$$V_{C2}=V_{C1}=\frac{1}{2}V_{Ceq} \tag{6}$$

$$V_{C2}(t)=\frac{1}{2}V_{dc}(1-\cos(\omega_\circ t)) \tag{7}$$

$$\omega_\circ=\frac{1}{\sqrt{LC_{eq}}} \tag{8}$$

If the duration of this mode is equal to $\pi\sqrt{LC_{eq}}$ or greater, the inductor current becomes zero. At this time, one can turn off S_1 and S_2 and turn on S_3 and S_4 and can be written:

$$V_{C1,1}=V_{C2,1}=V_{dc} \tag{9}$$

$V_{C1,1}$ and $V_{C2,1}$ are the voltage of C_1 and C_2 at the end of this step.

3.2. Switching mode 2:

With turning S_3 and S_4 on:

$$V_{C1}(t) = -2V_{dc}(1-\cos(\omega_{\circ}'t)) + V_{C1,1} \tag{10}$$

$$\omega_{\circ}' = 1/\sqrt{LC_1} \tag{11}$$

Equivalent capacity in this mode is C_1, so after the time interval $t=\pi\sqrt{LC_1}$, inductor current gets zero and one can turn S_3 and S_4 off and S_1 and S_2 on.

$$V_{C1,2} = -3V_{dc} \tag{12}$$

$$V_{C2,2} = V_{dc} \tag{13}$$

$V_{C1,2}$ and $V_{C2,2}$ are the voltage of C_1 and C_2 at the end of this step in the above equations.

3.3. The second switching mode 1:

When S1 and S2 turn on again, it can be written:

$$V_{C2}(t) = \frac{3}{2}V_{dc}(1-\cos(\omega_{\circ}t)) + V_{dc} \tag{14}$$

It is clear, switching in the circuit occurs at zero-current and at the end of this step:

$$V_{C2,3} = 4V_{dc} \tag{15}$$

$V_{C2,3}$ shows the final voltage of C_2. Capacitor voltage will remain constant and inductor current will remain zero until pulse is applied to the load.

3.4. Design Considerations

The energy of the output pulse is obtained from the following equation:

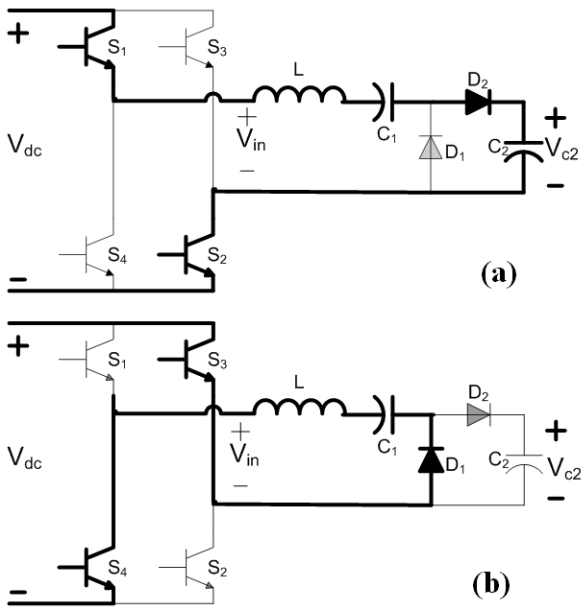

Figure 7. Switching mode of proposed topology a) mode1 b) mode 2

$$E_{pulse} = \frac{1}{2} C_2 (V_{C2,3} - V'_{C2}) \tag{16}$$

Where E_{pulse} is the energy in Joule and V'_{C2} is the remaining voltage of C_2. If all the energy stored in the capacitor is discharge V'_{C2} will be zero. The capacitance of circuit is obtained form (16) due to the amount of energy required per pulse. For the output frequency, it can be written:

$$f_{max} = \frac{1}{2\pi\sqrt{C_{eq1}L} + \pi\sqrt{C_{eq2}L} + T_{pulse} + T_{delay}} \tag{17}$$

Where f_{max} is the maximum output frequency in Hz, C_{eq1} and C_{eq2} are the equivalent capacity in the first mode and second mode, T_{pulse} is the pulse duration in second and T_{delay} is the delay time in switching. Inductor L must be selected according to output frequency and (17). But in the practice, it should be considered that the frequency may be different from than expected because of natural tolerance in the nominal value of inductors and capacitors. Furthermore, the parasitic resistance may increase the time required to the current for reaching zero [19].

TABLE I. THE VALUE OF ELEMENT USED IN THE SIMULATION

V_{dc}	L	C_1	C_2
100 v	**10mH**	**2 uF**	**2 uF**

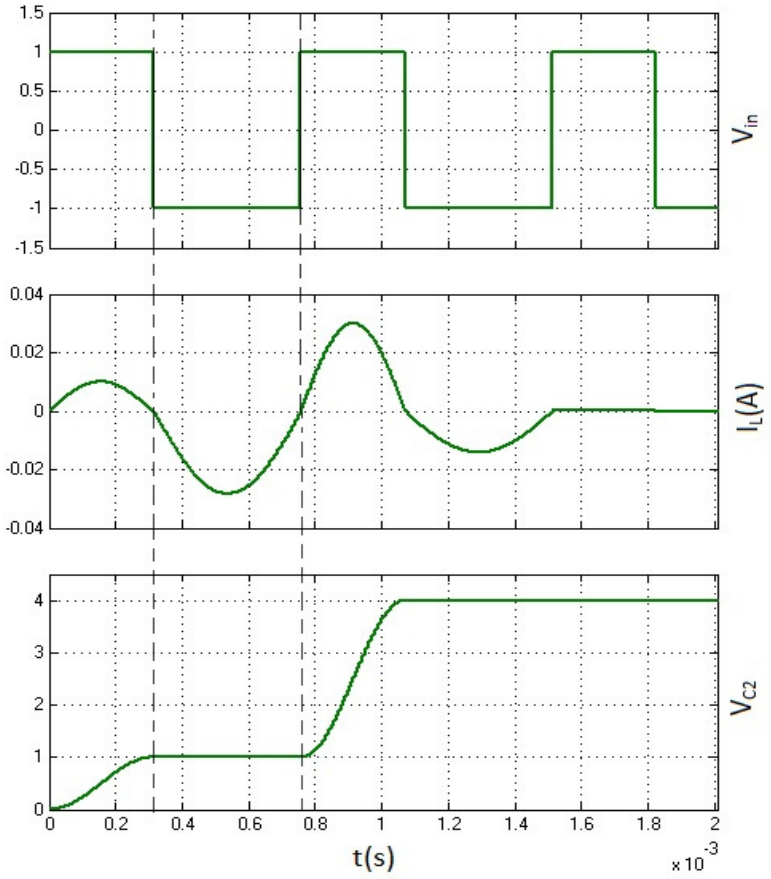

Figure 8. Capacitor voltage and inductor current of proposed topology (Capacitor voltage divided by the input voltage and plotted)

4. Simulation and Experimental Result

To evaluate the performance of the proposed topology, the values in Table 1 were used for simulation in MATLAB/SIMULINK. Simulation results for the inductor current and the capacitor voltage are shown in Fig. 8. A simple CDVM circuit that is fed by Sinusoidal voltage, a simple CDVM that is fed by full-bridge inverter and, a simple CDVM that connected to a resonant circuit also is simulated. The results of V_{C2} are shown in Fig. 9. The Capacitor voltage divided by the maximum input voltage and plotted.

Due to the added capacitor in resonant LC circuit and by considering CDVM values as constant, the calculation of frequency and resonance time will change and the resonance time will be a little longer. As is clear from the results, the response of the proposed converter is faster than all the models (except in CDVM fed by FB) and its output voltage is higher than the first two converters but less than a third converter.

Fig. 10 shows the inductor current in CDVM fed by LC. It is clear that if switching continued after the voltage reached maximum value, current will not be zero.

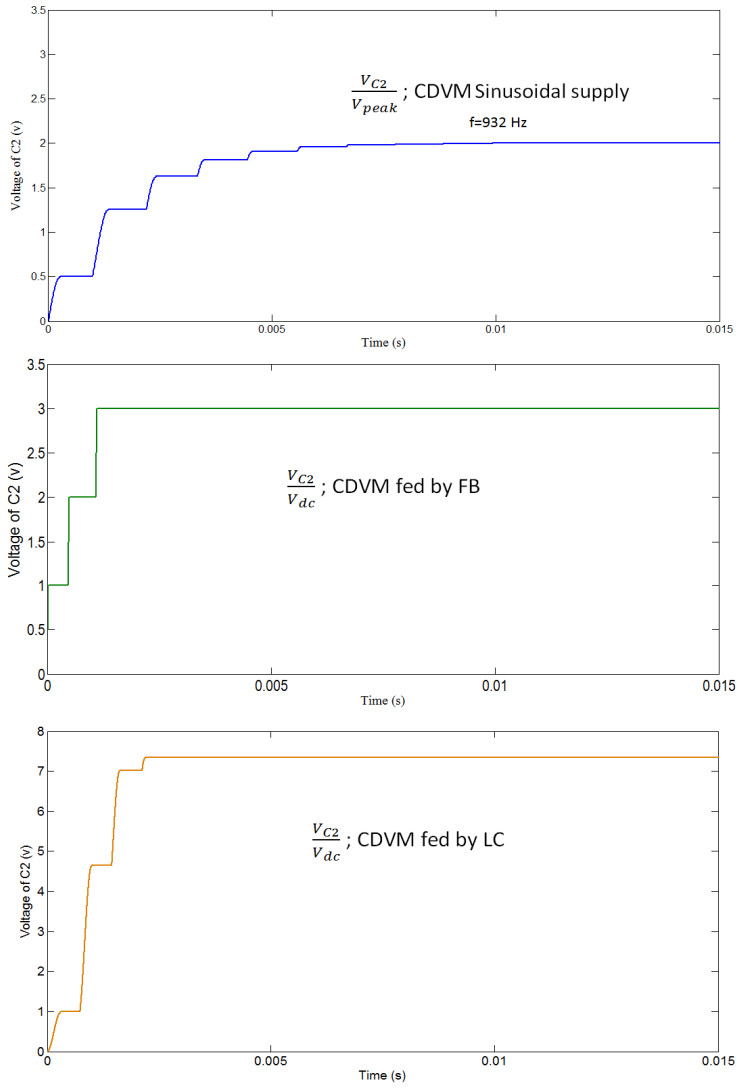

Figure 9. Simulation result for tree type CDVMs

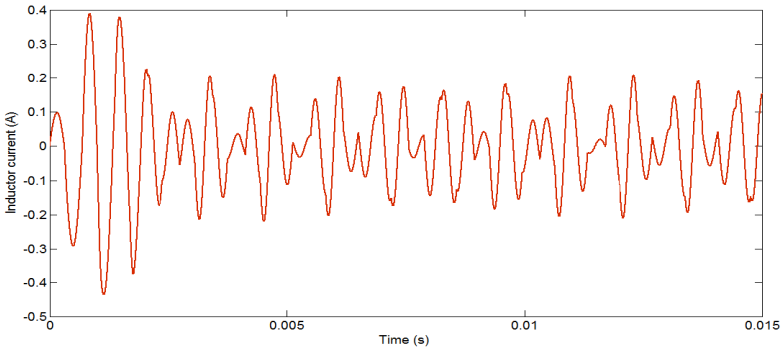

Figure 10. Inductor current in CDVM fed by LC circuit

TABLE II. THE SPECIFICATIONS OF PROTOTYPE

Input voltage	*C1*	*C2*	*L*	*Load*
100 V	**1 µF**	**1 µF**	**900 µH**	**12 Ω**

A simple experimental prototype of one-stage CDVM is implemented to study the proposed configuration practically. The prototype consists of a DC power supply, a full-bridge converter, an inductor, the one-stage CDVM, MOSFET drivers, isolated DC-DC converters for MOSFET drivers, an IGBT with a resistance load (10Ω, 250W) and a microcontroller board. In the full-bridge converter, common low rating MOSFETs are used as switches. In practice circuits for MOSFET drivers, full-bridge converters, and controller can be designed very compact. The specifications of the circuit are listed in Table 2.

The experimental results for the first cycle of inductor current and V_{C2} are shown in Fig. 11. Fig. 12 shows the inductor current, V_{C2}, and output voltage in steady state when the generator operates at about 2.78 kHz with a resistance load. As is clear from the results, the inductor current and the capacitor voltage are different from the first cycle to the next cycle because of the initial values of capacitor voltage, but the final voltage is the same in all cycles.

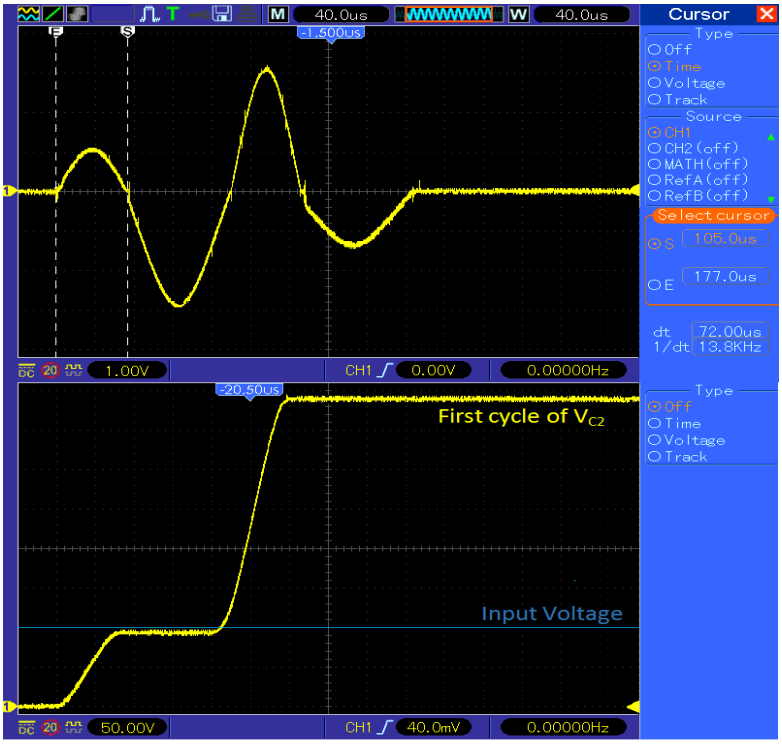

Figure 11. Experimental results in the first cycle

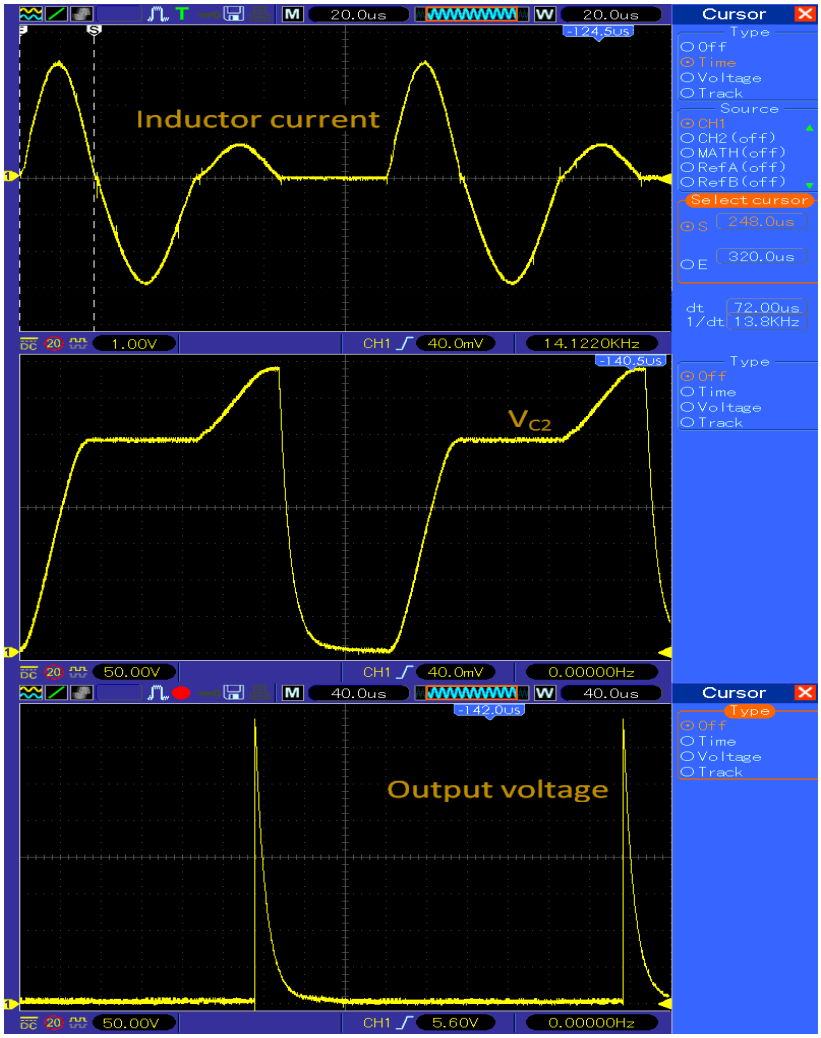

Figure 12. The experimental results in the steady state

The resonant period in the experimental is larger than expected about 7% because of natural tolerance in the nominal value of inductors and capacitors and the parasitic resistance. Although, because of the value selected for the inductor and capacitor in this prototype, damping factor is very small and the impact of parasitic resistance is negligible. The output voltage is smaller than expected because of non-ideal specifications of elements such as forward voltage of diodes and resistance in the circuit. The energy of each pulse is 0.072 joules and the input power rating of the prototype is 225 W. the efficiency of this prototype is about 90%.

5. Conclusion

In this paper, a new topology of CDVM converter has been proposed for pulse power applications, based on the resonance circuit. The use of resonance can improve switching performance at the higher output voltage. Simulation results show the improvement in performance of proposed circuit compared to conventional CDVM as well as experimental tests on a prototype setup have verified the capability of this topology in performing desired duties. Compare to the proposed circuit with CDVM circuit connected to an LC resonant network, the output voltage is reduced and the response is faster. Moreover, there is no need to additional capacitor in LC circuit. For isolation a transformer can be used in the topology.

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